

Dual N- and P-Channel 30-V (D-S) MOSFET

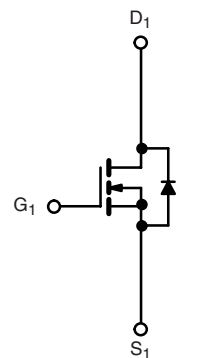
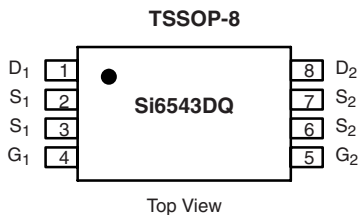
PRODUCT SUMMARY			
	V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)
N-Channel	30	0.065 at V _{GS} = 10 V	± 3.9
		0.095 at V _{GS} = 4.5 V	± 3.1
P-Channel	- 30	0.085 at V _{GS} = - 10 V	± 2.5
		0.19 at V _{GS} = - 4.5 V	± 1.8

FEATURES

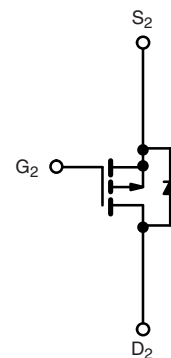
- Halogen-free Option Available



RoHS*
COMPLIANT



N-Channel MOSFET



P-Channel MOSFET

Ordering Information: Si6543DQ-T1
Si6543DQ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V _{DS}	30	- 30	V
Gate-Source Voltage	V _{GS}	± 20	± 20	
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	± 3.9	± 2.5
		T _A = 70 °C	± 3.1	± 2.1
Pulsed Drain Current	I _{DM}	± 20	± 20	A
Continuous Source Current (Diode Conduction) ^a	I _S	1.25	- 1.25	
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	1.0	
		T _A = 70 °C	0.64	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R _{thJA}	125	°C/W

Notes:

a. Surface Mounted on FR4 board, t ≤ 10 s.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>.

* Pb containing terminations are not RoHS compliant, exemptions may apply.

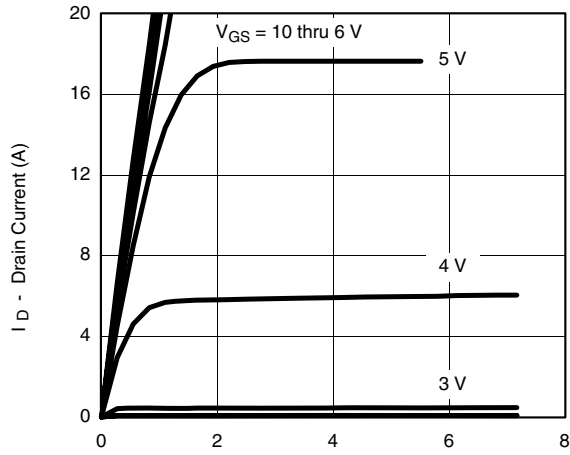
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	N-Ch	1.0			V
		$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	P-Ch	-1.0			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$	N-Ch P-Ch			± 100 ± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	N-Ch			25	
		$V_{DS} = -30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	P-Ch			-25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	N-Ch	15			A
		$V_{DS} \geq -5\text{ V}, V_{GS} = -10\text{ V}$	P-Ch	-15			
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 3.9\text{ A}$	N-Ch		0.043	0.065	Ω
		$V_{GS} = -10\text{ V}, I_D = 2.5\text{ A}$	P-Ch		0.066	0.085	
		$V_{GS} = 4.5\text{ V}, I_D = 3.1\text{ A}$	N-Ch		0.075	0.095	
		$V_{GS} = -4.5\text{ V}, I_D = 1.8\text{ A}$	P-Ch		0.125	0.19	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 3.9\text{ A}$	N-Ch		7		S
		$V_{DS} = -15\text{ V}, I_D = -2.5\text{ A}$	P-Ch		5		
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.25\text{ A}, V_{GS} = 0\text{ V}$	N-Ch		0.8	1.2	V
		$I_S = -1.25\text{ A}, V_{GS} = 0\text{ V}$	P-Ch		0.8	-1.2	
Dynamic^b							
Total Gate Charge	Q_g	N-Channel $V_{DS} = 10\text{ V}, V_{GS} = 10\text{ V}, I_D = 3.9\text{ A}$	N-Ch		9.8	15	nC
Gate-Source Charge	Q_{gs}		P-Ch		8.7	15	
Gate-Drain Charge	Q_{gd}	P-Channel $V_{DS} = -10\text{ V}, V_{GS} = -10\text{ V}, I_D = -2.5\text{ A}$	N-Ch		2.1		
			P-Ch		1.9		
Turn-On Delay Time	$t_{d(on)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_G = 6\text{ }\Omega$	N-Ch		9	15	ns
			P-Ch		7	15	
Rise Time	t_r	P-Channel $V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$ $I_D \cong -1\text{ A}, V_{GEN} = -10\text{ V}, R_G = 6\text{ }\Omega$	N-Ch		6	18	
			P-Ch		9	18	
Turn-Off Delay Time	$t_{d(off)}$	N-Channel $V_{DD} = 10\text{ V}, R_L = 10\text{ }\Omega$	N-Ch		18	27	
			P-Ch		14	27	
Fall Time	t_f	P-Channel $V_{DD} = -10\text{ V}, R_L = 10\text{ }\Omega$	N-Ch		6	15	
			P-Ch		8	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.25\text{ A}, dl/dt = 100\text{ A}/\mu\text{s}$	N-Ch		48	80	
		$I_F = -1.25\text{ A}, dl/dt = 100\text{ A}/\mu\text{s}$	P-Ch		46	80	

Notes:

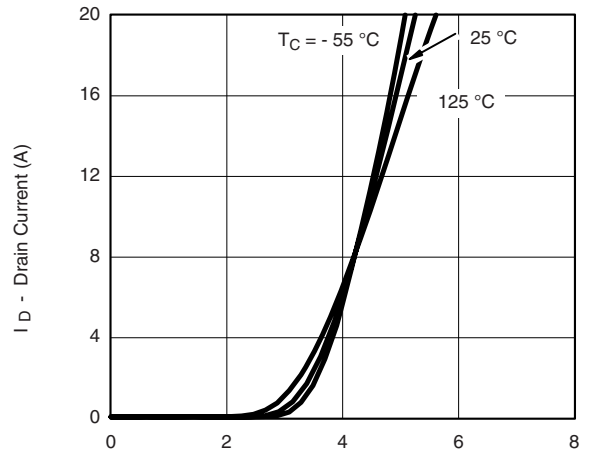
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

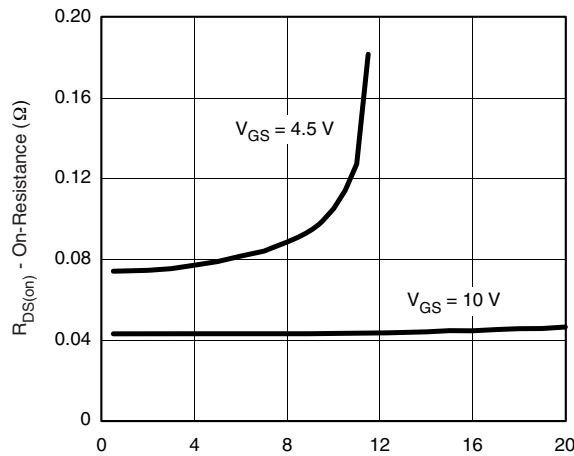
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



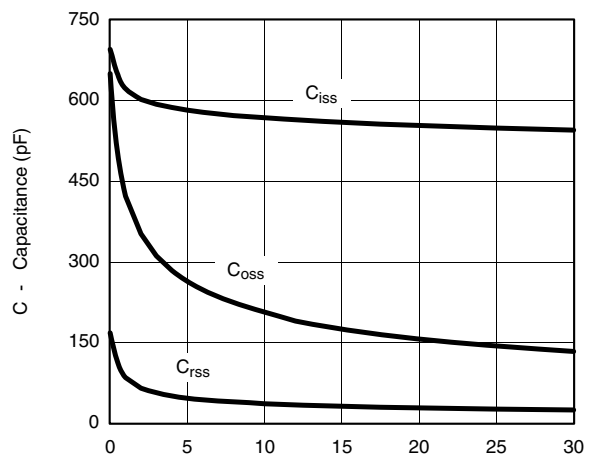
V_{DS} - Drain-to-Source Voltage (V)
Output Characteristics



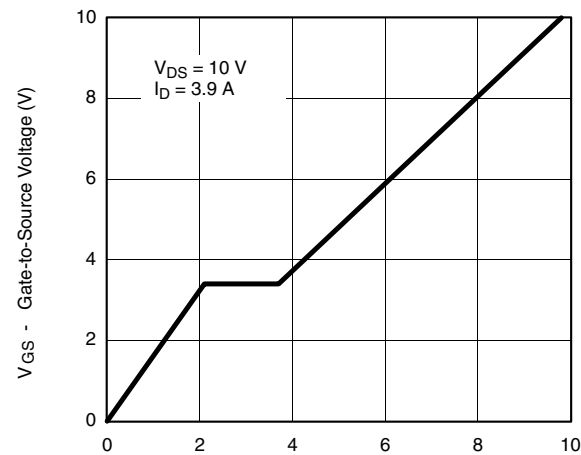
V_{GS} - Gate-to-Source Voltage (V)
Transfer Characteristics



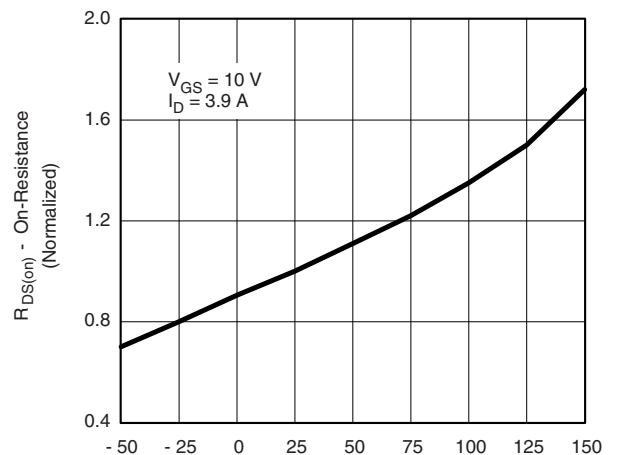
I_D - Drain Current (A)
On-Resistance vs. Drain Current



V_{DS} - Drain-to-Source Voltage (V)
Capacitance

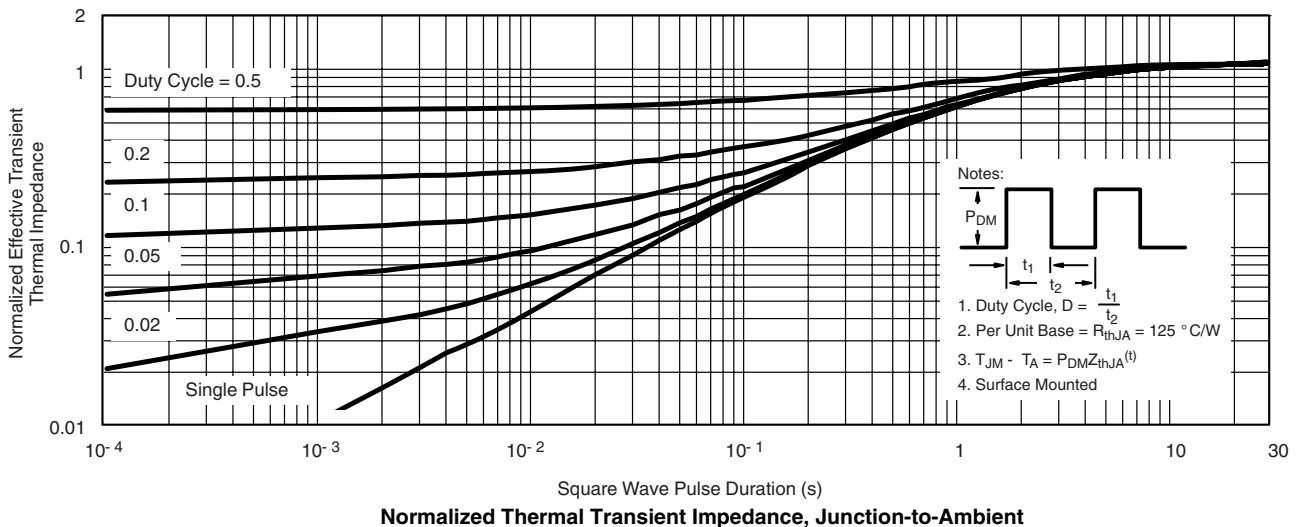
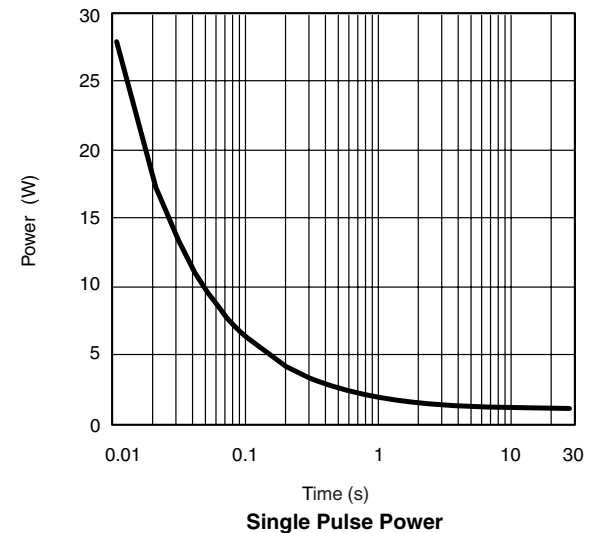
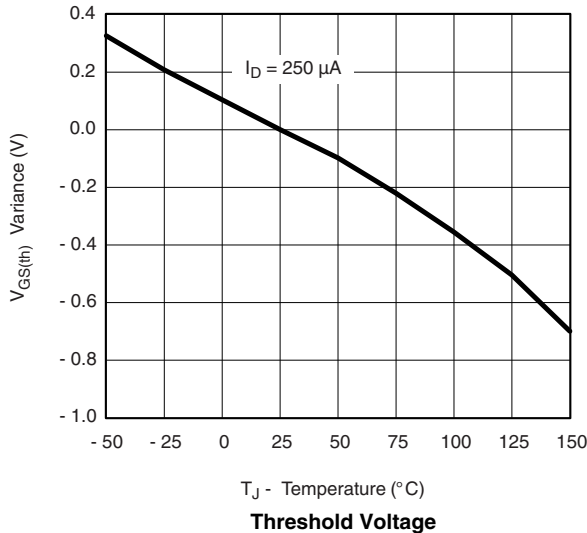
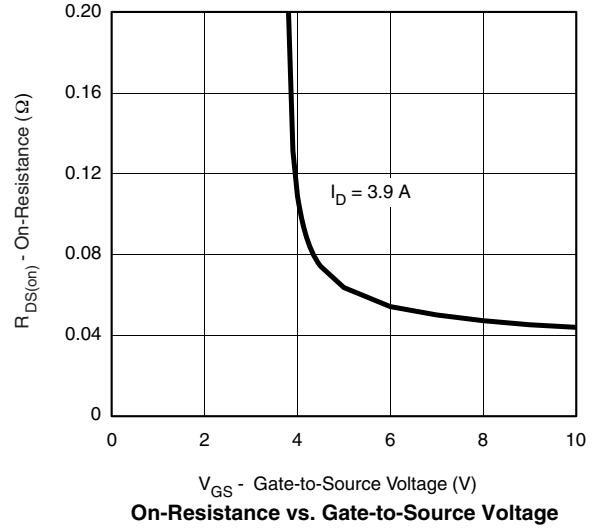
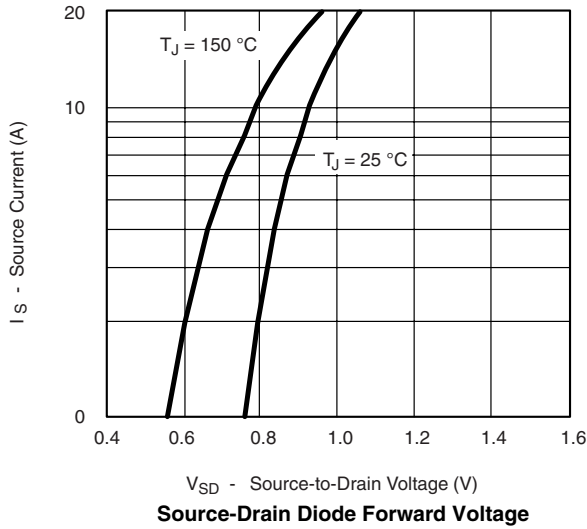


Q_g - Total Gate Charge (nC)
Gate Charge

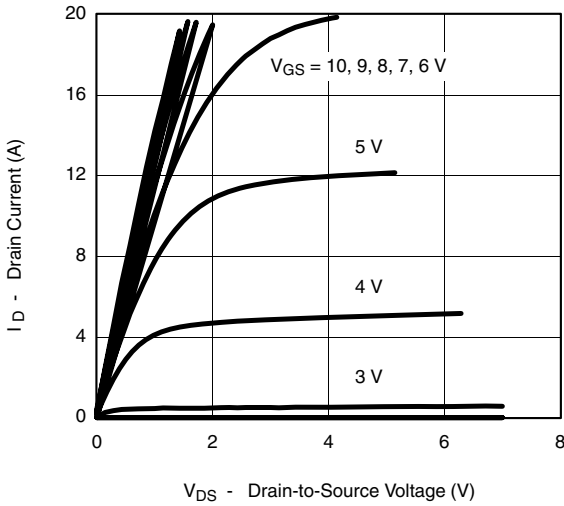


T_J - Junction Temperature ($^\circ\text{C}$)
On-Resistance vs. Junction Temperature

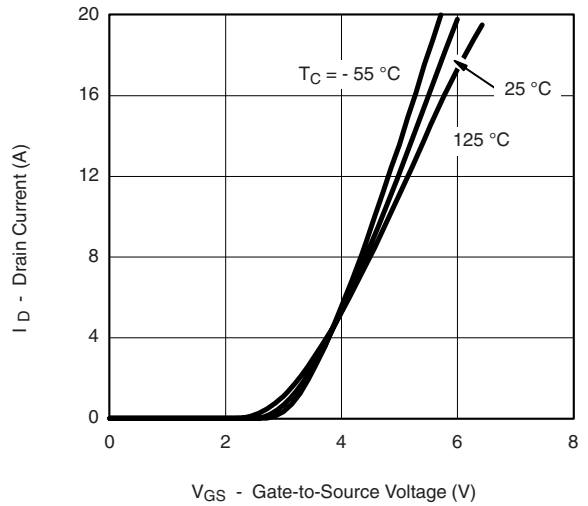
N-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



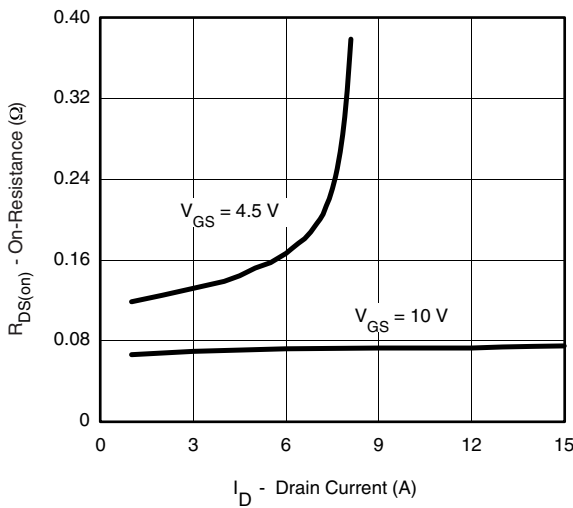
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



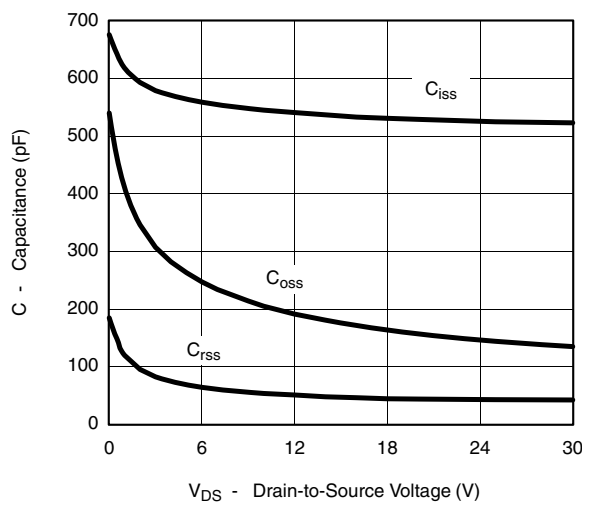
V_{DS} - Drain-to-Source Voltage (V)
Output Characteristics



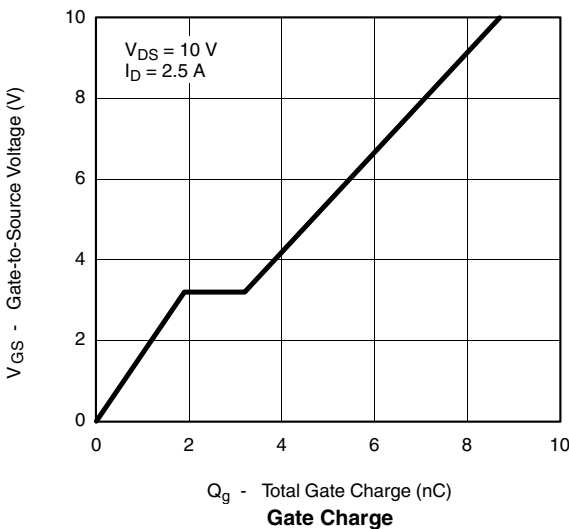
V_{GS} - Gate-to-Source Voltage (V)
Transfer Characteristics



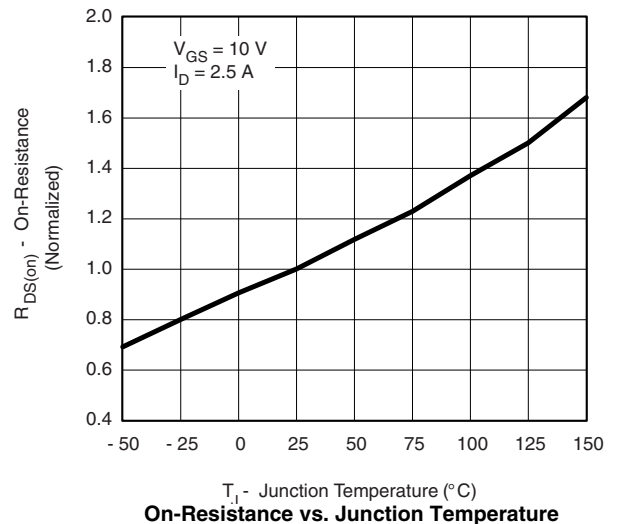
I_D - Drain Current (A)
On-Resistance vs. Drain Current



V_{DS} - Drain-to-Source Voltage (V)
Capacitance

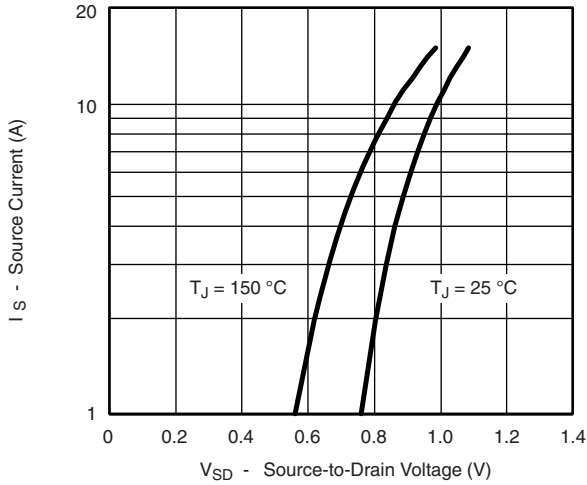


Q_g - Total Gate Charge (nC)
Gate Charge

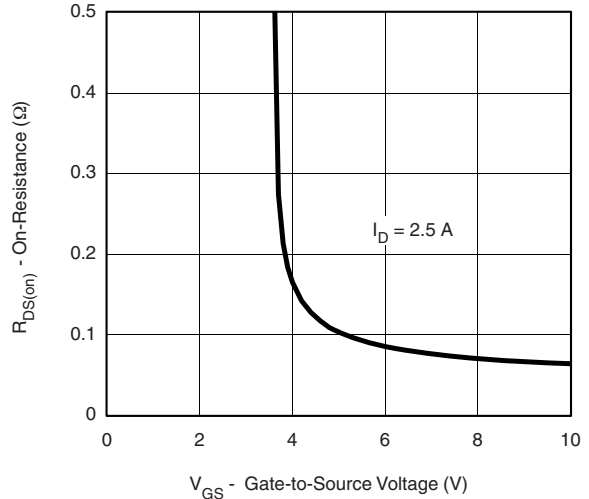


T_J - Junction Temperature ($^\circ\text{C}$)
On-Resistance vs. Junction Temperature

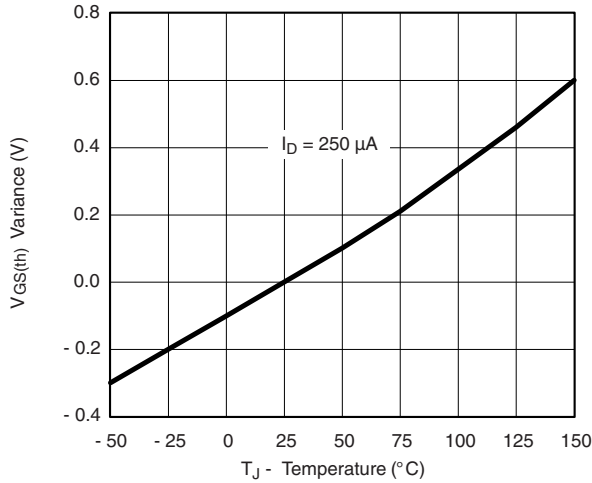
P-CHANNEL TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



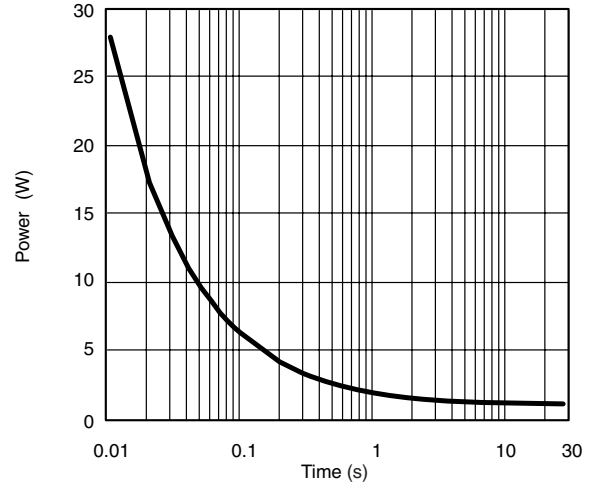
Source-Drain Diode Forward Voltage



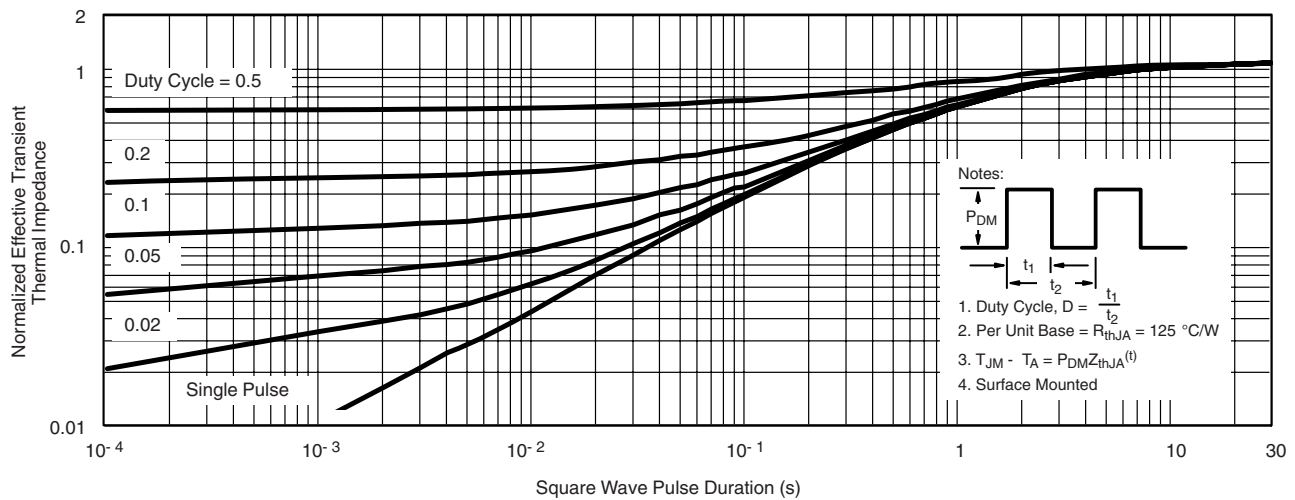
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

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